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U.S. PATENT APPLICATION

for

A DAMASCENE PROCESS FOR A T-SHAPED GATE ELECTRODE

Inventors: Ramkumar Subramanian
Christopher F. Lyons
Marina V. Plat
Bhanwar Singh

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CROSS REFERENCE TO RELATED PATENT APPLICATIONS

[0001] The present application is a continuation-in-part of U.S. Application Serial No. 09/620,300, filed on July 26, 2000 entitled "T Gate Formation Using a Modified Conventional Poly Process" by Subramanian, et al.; U.S. Application Serial No. 09/643,343, filed on August 22, 2000, entitled "Y Gate Formation Using Damascene Processing" by Subramanian, et al.; U.S. Application Serial No. 09/620,145, filed on July 20, 2000 entitled "T Gate Formation Using Modified Damascene Processing with Two Masks", by Subramanian, et al.; U.S. Application Serial No. 09/643,611, filed on August 22, 2000 entitled "T or T/Y Gate Formation Using Trim Etch Processing", by Subramaian, et al.; U.S. Application Serial No. 09/619,789, filed on July 20, 2000 entitled "Damascene T-Gate Using a RELACS Flow", by Subramanian, et al; and U.S. Application Serial No. 09/619,836, filed on July 20, 2000 entitled "Damascene T-Gate Using a Spacer Flow", by Subramanian, et al. All assigned to the Assignee of the present application.

FIELD OF THE INVENTION

[0002] The present invention relates generally to an integrated circuit (IC) and the fabrication of an integrated circuit. More particularly, the present invention relates to an integrated circuit having transistors with gate conductors having reduced resistance.

BACKGROUND OF THE INVENTION

[0003] Generally, it is desirous to manufacture smaller transistors to increase the component density on an integrated circuit. As transistors are reduced in size (CMOS scaling), the demands on lithographic tools have increased. Lithographic tools are utilized to form structures on the integrated circuit. For example, lithographic tools can be utilized to define gate conductors, conductive lines, vias, doped regions, and other structures associated with an integrated circuit.

[0004] In one type of conventional fabrication process, a photoresist is lithographically patterned by providing electromagnetic radiation such as ultraviolet light through an overlay. A conventional lithographic system is generally utilized to project the pattern to the photoresist material or layer. The photoresist material may be either a positive or a negative photoresist layer.

[0005] As the size of features on the integrated circuit reach sizes below 100 and even 50 nanometers, lithographic techniques are unable to precisely and accurately define the feature. For example, it is frequently desirous to reduce the width of the gate (the gate length) associated with a transistor. Future designs of transistors could require a gate conductor having a width of less than 50 nm.

[0006] In the case of a positive photoresist material or layer, the light causes photochemical reaction in the photoresist layer. The photoresist layer is removable with a developer solution at the portions of the photoresist that are exposed to light through a mask. The photoresist layer is developed to clear away those portions. An integrated circuit feature, such as a gate, via, or interconnect, is etched or doped into the layer of material, and the remaining photoresist is removed. In the case of a negative photoresist material, the light causes the photoresist layer to

be removable with a developer solution at portions of the photoresist layer that are not exposed to light through the mask.

[0007] Various types of photoresist materials are manufactured by a number of manufacturers. The photoresist material can include multiple photoresist films (i.e. a multi-level resist (MLR)). According to some conventional processes, the photoresist layer is provided over an anti-reflective coating (ARC), such as silicon nitride (Si_3N_4) or silicon oxynitride (SiON). The anti-reflective coating is disposed above the material which is to be processed.

[0008] Conventional processes have utilized a variety of resolution enhancement technologies for lithographically creating patterns which define lines and spaces. These processes include the use of phase shift masks, resist enhancement lithography assisted by chemical shrink (RELACS), the use of reflow operations and the use of ultrathin photoresist layers.

[0009] RELACS techniques by Clariant AZ utilizes a polymer with an R2 coating and R200 developer to shrink the size of contact holes. The RELACS process can use a coat, diffusion bake and rinse step after wafer patterning.

[0010] T-shaped gate conductors have been considered for future designs. T-shaped gate conductors can reduce the resistance associated with small gate lengths due to the large gate width at the top transistor and yet achieve densely packed transistors due to the small gate width at the bottom. Heretofore, T-shaped gate conductors have not been formed according to resolution enhancement.

[0011] Thus, there is a need for a method of making a novel transistor structure which is less susceptible to gate resistance and yet has an acceptable size. Further still, there is a need for a dual damascene method for manufacturing a gate structure. Even, further still, there is a need for a method of fabricating a gate structure which provides a gate

conductor having a width less than a width achievable by conventional lithographic techniques

SUMMARY OF THE INVENTION

[0012] An exemplary embodiment relates to a method of manufacturing an integrated circuit. The method includes providing a gate dielectric above a top surface of a substrate, providing a silicon and nitrogen containing layer above the gate dielectric layer, and providing an oxide layer above the silicon and nitrogen containing layer. The method also includes steps of selectively etching the oxide layer to form a first trench in the oxide layer, selectively etching the silicon and nitrogen containing layer to form a second trench in the silicon and nitrogen containing layer, and providing a gate conductor material in the first trench and second trench. The second trench is narrower than the first trench and disposed below the first trench.

[0013] Still another exemplary embodiment relates to a method of manufacturing an ultra-large scale integrated circuit. The integrated circuit includes a transistor with a T-shaped conductor. The method includes steps of providing a first layer above a substrate, providing an oxide layer on the first layer, forming a first trench in the oxide layer, forming a second trench in the first layer, and providing a gate conductor material in the first trench and the second trench to form the T-shaped conductor. The first layer is a silicon rich nitride layer or a silicon oxynitride layer. The second trench has a smaller width than the first trench.

[0014] Still another exemplary embodiment relates to a method of manufacturing a gate conductor for an integrated circuit. The method includes providing a first layer above a gate dielectric layer, forming an aperture in the first layer utilizing a RELACS process, filling the aperture with a gate conductor material, and removing the gate conductor material

above the first layer. The gate dielectric layer is disposed above the a substrate, and the first layer includes silicon oxynitride or silicon rich nitride.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0016] FIGURE 1 is a cross-sectional view of a portion of an integrated circuit including a transistor with a T-shaped gate electrode in accordance with an exemplary embodiment;

[0017] FIGURE 2 is a cross-sectional view of the portion of the integrated circuit illustrated in FIGURE 1, showing a gate dielectric deposition step and a silicon rich nitride or silicon oxynitride deposition step;

[0018] FIGURE 3 is a cross-sectional view of the portion of the integrated circuit illustrated in FIGURE 2, showing an oxide layer deposition step;

[0019] FIGURE 4 is a schematic cross-sectional view of the portion illustrated in FIGURE 3, showing a selective etching step;

[0020] FIGURE 5 is a cross-sectional view of the portion of the integrated circuit illustrated in FIGURE 4, showing an etching step;

[0021] FIGURE 6 is a schematic cross-sectional view of the portion of the integrated circuit illustrated in FIGURE 5, showing a gate conductor deposition step;

[0022] FIGURE 7 is a schematic cross-sectional view of the integrated circuit illustrated in FIGURE 6, showing a polishing step;

[0023] FIGURE 8 is a schematic cross-sectional view of the integrated circuit illustrated in FIGURE 7, showing an oxide layer removal step and a spacer formation step; and

[0024] FIGURE 9 is a schematic cross-sectional view of the integrated circuit illustrated in FIGURE 5, showing a RELACS processing step in accordance with another exemplary embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] With reference to FIGURE 1, a portion 10 of an integrated circuit (IC) includes a transistor 12 which is disposed on a semiconductor substrate 14, such as, a wafer. Semiconductor substrate 14 is preferably a bulk P-type silicon substrate including isolation structures 52. Alternatively, substrate 14 can be any type of IC substrate including a gallium arsenide (GaAs), germanium, or a semiconductor-on-insulator (SOI) substrate (e.g., a silicon-on-glass substrate).

[0026] Transistor 12 can be a P-channel or N-channel metal oxide semiconductor field effect transistor (MOSFET). Transistor 12 includes a gate structure 18, a source region 22, and a drain region 24. For an N-channel transistor, regions 22 and 24 are heavily doped with N-type dopants (e.g., $5x10^{19}$ – $1x10^{20}$ dopants per cubic centimeter). For a P-channel transistor, regions 22 and 24 are heavily doped with P-type dopants ($5x10^{19}$ - $1x10^{20}$ dopants per cubic centimeter). An appropriate dopant for a P-channel transistor is boron, boron diflouride, or iridium, and an appropriate dopant for an N-type transistor is arsenic, phosphorous, or antimony.

[0027] Source and drain regions 22 and 24 can be provided with extensions. Preferably, ultra-shallow extensions (e.g., junction depth is less than 250Å), preferably 10-25 nanometers (nm)) are integral with regions 22 and 24. The source and drain extensions can be disposed partially underneath gate structure 18.

[0028] A channel region 41 underneath gate structure 18 separates regions 22 and 24. Region 41 can be doped according to device

parameters. For example, region 41 can be doped according to a super steep retrograded well region.

[0029] Gate stack or structure 18 includes a T-shaped conductor 37, and a gate dielectric layer 34. T-shaped conductor 37 has a top portion 39 and a bottom portion 36. The width of channel region 41 (the gate length) is approximately the width of bottom portion 36 of gate conductor 37.

[0030] Bottom portion 36 has a smaller width than top portion 39. Preferably, the width of the bottom portion 36 is 250-1500 Å and the width of top portion 39 is 400-2000 Å. Bottom portion 36 is preferably 1000-2000 Å in height and top portion 39 is preferably 500-1000 Å in height. Gate structure 18 has a total height of 1000-3000 Å.

[0031] Top portion 39 of T-shaped gate conductor 37 and regions 22 and 24 can be silicided. Contacts and interconnects can be electrically coupled to top portion 39 and regions 22 and 24.

[0032] Dielectric layer 34 is preferably a 15 to 30 nm thick thermally grown silicon dioxide layer. Alternatively, layer 34 can be a silicon nitride (Si_2N_4) layer. Dielectric layer 34 can be comprised of a high-k dielectric material such as a 2-10 nm thick layer of tantalum pentaoxide (Ta_2O_5), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2) or other material having a dielectric constant (k) over 8.

[0033] T-shaped gate conductor 37 is preferably a semiconductive material. According to one embodiment, conductor 37 can be a polysilicon, germanium, or a silicon/germanium material. T-shaped gate conductor 37 is also preferably heavily doped with an N-type dopant, such as phosphorous (P), arsenic (As) or other dopant. Alternatively, gate conductor 37 can be doped with a P-type dopant, such a boron (B), boron diflouride (BF_2), or other dopants.

[0034] T-shaped gate conductor 37 can be implanted with dopants or with other semiconductive materials or can be an in situ doped material.

According to another embodiment, T-shaped conductor 37 can be a metal material.

[0035] Spacers 26 can abut lateral sides of bottom portion 36 of gate conductor 37. Spacers 26 can be located between portion 39 and gate dielectric layer 34. In addition, spacers 26 can be located below a bottom surface of top portion 39 of gate conductor 37. Preferably, spacers 26 are 1000-2000 Å high

[0036] Spacers 26 are preferably a silicon oxynitride (SiON) material or a silicon rich nitride material (SiRN). Alternatively, spacers 26 can be other insulative materials like SiO_2 or SiN. Preferably, spacers 26 are formed in accordance with the process described below with reference to FIGURES 1-9.

[0037] Transistor 12 can be an N-channel or a P-channel field effect transistor, such as, a metal oxide semiconductor field effect transistor (MOSFET). Transistor 12 is at least partially covered by insulative layer 48 and is preferably part of an ultra-large scale integrated (ULSI) circuit that includes one million or more transistors.

[0038] With reference to FIGURES 1-9, an advantageous process of forming transistor 12 is described below. The process advantageously provides a novel damascene fabrication flow in which a T-shaped gate conductor is formed. Preferably, a RELACS process is utilized to form bottom portion of 36 of gate conductor 37.

[0039] With reference to FIGURE 2, substrate 14 includes top surface 27 having gate dielectric layer 34 disposed thereon. Preferably, gate dielectric layer 34 is a silicon dioxide (SiO_2) layer formed by chemical vapor deposition (CVD) or thermal growth. Alternatively, layer 34 can be other materials including silicon nitride or high-K dielectric materials.

[0040] Substrate 14 can include isolation regions 52 and source and drain regions 22 and 24 (FIGURE 1) before layer 34 is provided. The

formation of regions 22 and 24 and other transistor structures unrelated to gate structure 18 is beyond the scope of this disclosure.

[0041] After layer 34 is deposited, a layer 40 is deposited above layer 34. Layer 40 is preferably a silicon and nitrogen containing layer. In one embodiment, layer 40 can be a silicon oxynitride (SiON) layer. In an alternative embodiment, layer 40 can be a silicon rich nitride layer (SiRN). Layer 40 is preferably 2000 Å thick and deposited by chemical vapor deposition (CVD).

[0042] With reference to FIGURE 3, an oxide layer 42 is provided above layer 40. Layer 42 can be deposited by chemical vapor deposition (CVD). Preferably, layer 42 has a thickness of 500 and includes silicon dioxide (SiO_2). Alternatively, layer 42 can be grown above layer 40. Layer 40 preferably has different etch characteristics than layer 42.

[0043] With reference to FIGURE 4, layer 42 is selectively etched or removed to provide a first trench 44 in layer 42. Preferably, trench 44 has a width of 500 Å associated with the width of top portion 39 of gate conductor 37 (FIGURE 1). Trench 44 exposes a top surface 45 of layer 40.

[0044] Layer 42 is preferably patterned to form trench 44 in accordance with a dark field mask. A conventional photolithographic process via the dark field mask can pattern a photoresist layer above layer 42. An etching step selective to silicon oxide with respect to silicon oxynitride or silicon rich nitride can be used to form aperture or trench 44. After etching, the pattern photoresist mask can be removed from above layer 42.

[0045] With reference to FIGURE 5, layer 40 is selectively removed or etched to form a trench 46. Trench 46 preferably has a width smaller than the width of trench 44. In one embodiment, the width of trench 46 is 350 Å or 70 percent of the width of trench 44. Trench 46 can be formed in a conventional photolithographic process similar to the process

used to form trench 44 or in a RELACS process as described with reference to FIGURE 9. Trench 46 extends to dielectric layer 34.

[0046] According to the conventional photolithographic process, layer 42 and exposed surfaces 48 of trench 44 are covered with a photoresist layer. The photoresist layer is selectively patterned. Layer 40 is etched in accordance with the patterned photoresist material to form trench 46. Layer 40 can be etched using a process selective to silicon oxynitride or silicon rich nitride with respect to silicon dioxide. Preferably, a dry etching process is utilized.

[0047] With reference to FIGURE 6, after trenches 44 and 46 are formed, a gate conductor material 54 is provided in trenches 44 and 46. Preferably, gate conductor material 54 is deposited as a conformal layer. A 3000-5000 Å thick layer of polysilicon (doped or undoped) can be deposited by CVD and polished back to final thickness. In another embodiment, a refractory metal or other gate conductor material can be utilized as material 54.

[0048] With reference to FIGURE 7, material 54 is polished to leave gate conductor 37 in trenches 44 and 46 (FIGURE 6). Alternatively, other removal processes can be utilized including etching techniques.

[0049] With reference to FIGURE 8, layer 42 can be removed in a dry etching process. After layer 42 is removed, layer 40 can be removed. In one embodiment, layer 40 can be completely removed by dry etching. Portions of layer 34 can also be removed by wet or dry etching.

[0050] According to another embodiment, layer 42 can be selectively removed using top portion 39 of gate conductor 37 (material 54 within trench 44) as an etch mask to leave spacers 26 between conductor 36 and substrate 14. In this embodiment, spacers 26 include silicon oxynitride or silicon rich nitride (the material of layer 40 FIGURES 2-7).

[0051] With reference to FIGURE 1, source and drain regions 22 and 24 can be formed if they have not already been formed. In accordance with

conventional processes, further conventional processes can be utilized to provide insulative layer 48, contacts, vias and other interconnects.

[0052] With reference to FIGURE 9, a resist enhancement lithography assisted by chemical shrink (RELACS) process can be utilized to form aperture or trench 46. The RELACS process is begun after trench 44 is formed as described with reference to FIGURE 4.

[0053] In FIGURE 9, after trench 44 (not shown in FIGURE 9) is formed, a photoresist layer 80 is provided above layer 42. Layer 80 can be spun on to layer 42 as a 2000-6000 Å thick layer. Layer 80 can be a photoresist material such as Shipley's UV210 for use at 248 nm lithography or Sumitomo's PAR707 for use at 193 nm or other suitable resists. Photoresist layer 80 is preferably provided on a top surface 82 of layer 42 and sidewalls 84 of layer 42. Layer 80 is patterned to have an aperture with a width smaller than trench 44 and larger than trench 46.

[0054] After layer 80 is provided, a RELACS polymer 86 is provided over layer 80. Preferably, after layer 80 is patterned, RELACS polymer 86 is spread onto and around resulting in the formation as shown in FIGURE 9. The preferred method for spreading RELACS polymer 86 onto layer 80 is by spin coating. Other methods of spreading RELACS polymer 86 are contemplated. For example, a spray coat process may apply polymer 86.

[0055] Polymer 86 covers patterned photoresist layer 80 and bonds with layer 80. Bonding takes place on a top surface 92 of layer 80 and sidewalls 94 of layer 80. Bonding can be due to cross linking of polymer 86 with surface 92 and sidewalls 94. Polymer 86 can be a 10-70 % of the resist thickness.

[0056] Polymer 86 is removed in a blanket etch process from surface 92 of photoresist layer 80. Preferably, the blanket etch is an anisotropic etch. The anisotropic etch removes portions of polymer 86 from top

surface 92 and sidewalls 94. However, portions of polymer 86 remain disposed against sidewalls 94 of layer 80.

[0057] According to another embodiment, layer 86 can be removed in a chemical mechanical polishing (CMP) process. The CMP process removes polymer 86 from surface 92 and sidewalls 94 and allows polymer 86 to remain on sidewalls 94.

[0058] According to both embodiments, polymer 86 is left on sidewalls 84 and defines trench 46. The size of trench 46 can be controlled by the controlling the time in which polymer 86 is spread over patterned layer 80 (a longer spreading time results in wider RELACS polymer sidewall portions). Further, the removal chemistry and time can be varied to adjust the size defined by portions of polymer 86 on sidewalls 94.

[0059] Layer 40 is etched in accordance with the portions on sidewalls 94 to provide trench 46. Preferably, layer 40 is etched in a dry etching process. After etching trench 46, polymer 86, layers 82 and 80 can be completely stripped from portion 10.

[0060] According to another embodiment, conductor 36 is not T-shaped but instead has a rectangular cross section. According to such an embodiment, the method utilized to form transistor 12 discussed with reference to FIGURES 1-8 is utilized. However, steps related to the use of oxide in trench 44 are removed. Instead, trench 46 is formed using a RELACS process and gate conductor material 54 is deposited only in trench 46 to form a gate conductor 37 including only bottom portion 36. According to this process, a small cross-sectional gate for gate conductor 37 is achieved (e.g., smaller than available according to conventional lithographic techniques).

[0061] It is understood that while preferred embodiments and specific examples are given, they are for the purpose of illustration only and are not limited to the precise details disclosed. For example, although specific RELACS processes are discussed, other etching techniques can

be utilized. Various modifications may be made in the details within the scope and range of equivalents of the claims without departing from what is claimed.